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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/918,511	DAI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- Th MAILING DATE of this communication appears on the c ver sh et with th c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9, 11-21, 23,25-31-33, and 35-37 rejected under 35 U.S.C. 102(b) based upon a public use or sale of the invention. Zavracky et al. Patent Number 5705424.

Zavracky discloses:

(See FIGS. 1A-1D, 8A-8C, 9A-9D; col. 3 lines 49-67 through col. 4 lines 1-7; col. 5 lines 42-55 and lines 62-67 continued through col. 6 lines 1-5)

1. A method for manufacturing thin film transistor panel, at least, comprises following step:

provide a silicon substrate (8);

form a of transparent insulator (26) on the front surface of said silicon substrate;

form a plurality of thin film transistor structures and a plurality of corresponding transparent electrodes (250) on said transparent insulator;

bond a transparent substrate (24) onto the front surface of said silicon substrate;

remove said silicon substrate; and

etch said transparent insulator to expose said transparent electrode.

(See FIG. 12C; col. 4 lines 23-24; col. 6 lines 67 through col.7 line 1, and lines 31-36)

2. A method for manufacturing thin film transistor panel of claim 1, wherein said transparent insulator is SiO.

3. A method for manufacturing thin film transistor panel of claim 1, wherein said transparent insulator is SiN.

4. A method for manufacturing thin film transistor panel of claim 1, wherein the thickness of said transparent insulator is below one micrometer.

(See col. 4 lines 23-24)

5. A method for manufacturing thin film transistor panel of claim 1,wherein the material of said transparent electrode (44) is indium tin oxide.

(See col. 3 lines 53-54)

6. A method for manufacturing thin film transistor panel of claim 1, wherein said transparent substrate is glass substrate.

(See col. 7 lines 31-36)

7. A method for manufacturing thin film transistor panel of claim 1, wherein said transparent substrate is polymer substrate.

(See col. 3 lines 58-60)

9. A method for manufacturing thin film transistor panel of claim 1, wherein said the method for removing said silicon substrate includes etching process.

(See 8A-8C, 9A-9D; col. 5 lines 42-55 and lines 62-67 continued through col. 6 lines 1-5)

(See col. 4 lines 23-24; FIG.12C; col. 7 lines 31-36)

(See col. 6 lines 67 through col.7 line 1)

(See FIG 13A; col. 8 lines 45 (implied back matrix); col. 10 lines 8-13)

11. A method for manufacturing thin film transistor panel of claim 1, further comprises a step for forming a back matrix (500) on said thin film transistor structure before bonding said transparent substrate onto the front surface of said silicon substrate.

12. A method for manufacturing thin film transistor panel of claim 1, wherein the step

for forming said thin film transistor structure and said transparent electrode comprises:

form a transistor thin film and a transparent electrode on said transparent insulator;

form a gate insulator covering said transistor thin film and said transparent electrode;

form a gate electrode on said gate insulator corresponding to the position of said transistor thin film;

form an interlayer on said gate electrode and said gate insulator;

form a metal contact layer on said gate insulator; and

form a passivation layer (22) on said metal contact layer (46).

See 8A-8C, 9A-9D; col. 5 lines 42-55 and lines 62-67 continued through col. 6 lines 1-5)

(See col. 4 lines 23-24; FIG.12C; col. 7 lines 31-36)

(See col. 6 lines 67 through col.7 line 1)

13. A method for manufacturing thin film transistor panel of claim 12, wherein the material of said transistor thin film can be anyone of the group of polycrystal silicon (p-Si) , polycrstal germanium (p-Ge) - polycrystal silicon germanium (p-SiGe) - crystal silicon c-Si) , crystal germanium (c-Ge) , crystal silicon germanium (c-SiGe) .

14. A method for manufacturing thin film transistor panel of claim 12, further comprises a step of forming a color filter on said passivation layer.

15. A method for manufacturing thin film transistor panel, at lease, comprise following steps:

provide a silicon substrate;

form a transparent insulator on the front surface of said silicon substrate;

form a plurality of thin film transistor structures on said the transparent insulator;

bond a transparent substrate onto the front surface of said silicon substrate;

remove said silicon substrate; and

form a plurality of transparent electrodes corresponding to said thin film transistor structure on the bottom surface of said transparent insulator.

16. A method for manufacturing thin film transistor panel of claim 15, wherein said transparent insulator is SiO,

17. A method for manufacturing thin film transistor panel of claim 15, wherein said transparent insulator is SiN,.

See 8A-8C, 9A-9D; col. 5 lines 42-55 and lines 62-67 continued through col. 6 lines 1-5)

(See col. 4 lines 23-24; FIG.12C; col. 7 lines 31-36)

(See col. 6 lines 67 through col.7 line 1)

18. A method for manufacturing thin film transistor panel of claim 15, wherein the thickness of said transparent insulator is below one micrometer.

19. A method for manufacturing thin film transistor panel of claim 15, wherein the material of said transparent electrode is indium tin oxide.

20. A method for manufacturing thin film transistor panel of claim 15, wherein said transparent substrate is glass substrate.

21. A method for manufacturing thin film transistor panel of claim 15, wherein said transparent substrate is polymer substrate.

23. A method for manufacturing thin film transistor panel of claim 15, wherein said the method for removing said silicon substrate includes etching process.

25. A method for manufacturing thin film transistor panel of claim 15, further comprises process for forming a back matrix on said thin film transistor structure before bonding said transparent substrate onto the front surface of said silicon substrate.

26. A method for manufacturing thin film transistor panel of claim 15, wherein the steps for forming said thin film transistor comprises:

form a transistor thin film on said front surface of said transparent insulator;

form a gate insulator covering said transistor thin film and said transparent electrode;

form a gate electrode on said gate insulator corresponding to the position of said transistor thin film;

(See 8A-8C, 9A-9D; col. 5 lines 42-55 and lines 62-67 continued through col. 6 lines 1-5)

(See col. 4 lines 23-24; FIG.12C; col. 7 lines 31-36)

(See col. 6 lines 67 through col.7 line 1)

form an interlayer on said gate electrode and said gate insulator;

form a metal contact layer on said gate insulator; and

form a passivation layer on said metal contact layer.

27. A method for manufacturing thin film transistor panel of claim 26, wherein the material of said transistor thin film can be anyone from the group of polycrystal silicon (p-Si) , polycrystal germanium (p-Ge) - polycrystal silicon germanium (p-SiGe) , crystal silicon (c-Si) , crystal germanium (c-Ge) - crystal silicon germanium (c-SiGe).

(See col. 6 lines 40-42)

28. A method for manufacturing thin film transistor panel of claim 15, further comprises a step of forming a color filter on the bottom surface of said transparent insulator before forming said transparent electrode.

29. A method for manufacturing thin film transistor panel, at least, comprises following step:

provide a silicon substrate;

bond a transparent substrate onto the back of said silicon substrate;

reduce the thickness of said silicon substrate to form a layer of crystal silicon thin film;

form a plurality of thin film transistor structures on said crystal silicon thin film;

etch said thin film transistor structure layer and said crystal silicon thin film to form suitable pixel via;

(See 8A-8C, 9A-9D; col. 5 lines 42-55 and lines 62-67 continued through col. 6 lines 1-5)

(See col. 4 lines 23-24; FIG.12C; col. 7 lines 31-36)

(See col. 6 lines 67 through col.7 line 1)

form a planarization layer on said thin film transistor structure and said pixel via; and

form a plurality of transparent electrodes corresponding to the thin film transistor structures on said planarization layer.

30. A method for manufacturing thin film transistor panel of claim 29, wherein the thickness of said transparent insulator is below one micrometer.

31. A method for manufacturing thin film transistor panel of claim 29, wherein the material of said transparent electrode is indium tin oxide.

32. A method for manufacturing thin film transistor panel of claim 29, wherein said transparent substrate is glass substrate.

33. A method for manufacturing thin film transistor panel of claim 29, wherein said transparent substrate is polymer substrate.

35. A method for manufacturing thin film transistor panel of claim 29, wherein said the method for removing said silicon substrate includes etching process.

36. A method for manufacturing thin film transistor panel of claim 29, wherein the method for forming thin film transistor structure comprise:

form a source region and a drain region on said crystal silicon thin film;

form a gate insulator covering said transistor thin film and said transparent electrode; form a gate electrode on said gate insulator; form a interlayer on said gate electrode and said gate insulator; and form a metal contact layer on said gate insulator.

(See col. 6 lines 38-46

37. A method for manufacturing thin film transistor panel of claim 29, wherein the planarization layer is also color filter.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8, 10, 22, 24, 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky et al. Patent Number 5705424.

Zavracky discloses the claimed invention except for the use of a chemical mechanical polishing and forming an alignment mark, . It would have been obvious to on having ordinary skill in the art at the time of the invention was made to uses a chemical polishing method and an alignment mark based on the knowledge of conventional art, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 f.2d 272, 205 USPQ 215 (CCPA 1980). Therefore it would have also been obvious to one of ordinary skill in the art at the time of the invention based on the teachings of Zavracky to design an active matrix display (thin film transistor panel) with the motivation of designing pixel electrodes for an active matrix display device forming an array of transistor circuits. Finally, it would have been obvious based on a matter of conventional art to etch out at least the portion of the silicon substrate that is not connected to the transistor in order to deposit a transparent electrode in the exposed area to gain contact with the passivation layer for the purpose of conduction.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
July 10, 2002

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800